

PATENT APPLICATION
DOCKET NO.: 10012773-1

REMARKS

Claims 1-20 are pending, of which claims 1, 10, 14, and 20 are in independent form. Claim 10 is currently amended. New base claim 20 has been added by way of the present Response.

No new matter is introduced.

Favorable reconsideration of the present patent application as currently constituted is respectfully requested.

Regarding the Claim Objections and Allowable Subject Matter

Applicant gratefully appreciates the indication of allowable subject matter. In the outstanding Office Action, the Examiner has indicated that claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant has presented the allowable subject matter of claim 13 in new base claim 20. Accordingly, it is believed that base claim 20 is in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

In the pending Office Action, all pending claims 1-19 are rejected 35 U.S.C. §103(a) as being unpatentable over a number of

PATENT APPLICATION
DOCKET NO.: 10012773-1

references applied in various combinations: (i) claims 1-3, 14-16, and 19 over U.S. Patent No. 5,450,458 to Price et al. (the Price reference) in view of U.S. Patent No. 6,622,255 to Kurd et al. (the Kurd reference); (ii) claim 4 over the Price and Kurd references in further view of U.S. Patent No. 5,054,020 to Meagher (the Meagher reference); (iii) claims 5-9 and 17-18 over the Price and Kurd references in further view of U.S. Patent No. 6,396,322 to Kim et al. (the Kim reference); (iv) claims 10 and 12 over the Price and Meagher references; (v) claim 11 over the Price and Meagher references in further view of U.S. Patent No. 5,256,994 to Langendorf (the Langendorf reference); and (vi) claim 12 over the Price and Meagher references in further view of U.S. Patent No. 6,516,362 to Magro et al. (the Magro reference).

Analysis with respect to Base Claim 1:

The following comments were provided in particular reference to the §103 rejections of the base claim 1:

As per claim 1 Price discloses a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay

PATENT APPLICATION
DOCKET NO.: 10012773-1

compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals (figure 6 column 5 lines 41-44). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

Applicant respectfully traverses the pending §103 rejection of the base claim 1 as applied above and offers the following arguments in support. As set forth in the base claim 1, an embodiment of the present invention is directed to a SYNC pulse compensation apparatus that comprises, *inter alia*, a sampling compensation circuit operable to condition a SYNC pulse signal. The Price reference is directed to a digital information handling system that employs subsystems operating with different clock frequencies and which are capable of transferring data between one another. The applied language of the Price reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to a sampling compensation circuit operable to condition a SYNC signal. Rather, it merely discloses that a first

PATENT APPLICATION
DOCKET NO.: 10012773-1

synchronization circuit 136 generates a synchronization signal called SYNC READY to synchronize data transfer from Memory Controller 126 in a second subsystem clock environment to System Processor 124 in a first subsystem via System Processor Bus 128. Applicant respectfully submits that generation of SYNC READY signal does not anticipate or suggest conditioning a SYNC pulse as currently claimed. As set forth in the specification of the present patent application, conditioning of the SYNC pulse is performed by the sampling compensation circuit in order to remove certain anomalous conditions in the SYNC pulse, e.g., a lost SYNC pulse, a duplicate pulse condition, etc. See Specification at page 17, line 16 to page 18, line 11.

Moreover, as admitted in the pending Office Action, the Price reference does not disclose a jitter cycle delay compensation circuit as recited in the base claim 1. Application of the Kurd reference is of no avail, however, when applied as a secondary reference in combination with the Price reference in order to provide a basis for obviousness. It is well known that to establish obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined

PATENT APPLICATION
DOCKET NO.: 10012773-1

references must teach or suggest all the claim limitations. See MPEP §2143. Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention which involves, *inter alia*, (i) a sampling compensation circuit operable to condition a SYNC pulse signal; and (ii) a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap the SYNC pulse signal after a predetermined delay based on a skew difference between first and second clock signals. The Kurd reference is directed to digital clock skew detection and phase alignment between two digital clock signals that are copies of each other. See column 1, lines 11-24. As such, there is no teaching or suggestion in the Kurd reference with regard to a SYNC sampling compensation circuit operable to condition a SYNC pulse signal as discussed above. Figure 6 of the Kurd reference shows a circuit schematic of an application of a skew detection circuit for minimizing skew between different clock domains. Two separate frequency control circuits are provided, PLL1 606 and PLL2 608, which provide output clocks of different frequencies. Column 5, lines 41-47. A reference clock is split into two by a programmable delay circuit 504 and fed to separate

PATENT APPLICATION
DOCKET NO.: 10012773-1

inputs of the two PLLs. Each PLL adjusts the phase and/or frequency of its output signal to match that of the reference input. Column 5, lines 47-63. Based on the foregoing, Applicant respectfully submits that the skew detection circuit of the Kurd reference does not even remotely allude to a jitter cycle delay compensation circuit that is coupled to a SYNC sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap a conditioned SYNC pulse signal as currently claimed.

Accordingly, Applicant respectfully submits that the base claim 1 is allowable over the Price and Kurd references.

Analysis with respect to Base Claim 10:

The following comments were provided in particular reference to the §103 rejection of the base claim 10:

As per claim 10 Price discloses a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose that when the signal contains a plurality of logic lows during a predetermined time period, inserting a logic high condition at a select point in time. It is very well known and Meagher discloses that when the signal contains a plurality of a logic lows during a predetermined time period, inserting a logic high condition at a select point in time (figure 2, column 2 lines 30-31). Price and Meagher teachings

PATENT APPLICATION
DOCKET NO.: 10012773-1

are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 30-31).

Applicant respectfully traverses the pending §103 rejection of the base claim 10 and offers the following arguments in support. As currently constituted, the base claim 10 involves, *inter alia*, (i) sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and (ii) if the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing the anomalous condition by activating appropriate SYNC correct control logic. As discussed in detail hereinabove, the applied language of the Price reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to sampling a SYNC pulse signal. Further, the Price reference does not disclose or suggest removing of any anomalous condition in the sampled SYNC pulse signal by activating appropriate SYNC correct control logic, as currently claimed.

PATENT APPLICATION
DOCKET NO.: 10012773-1

The *Meagher* reference is directed to a scheme for converting an incoming asynchronous data signal into an outgoing synchronous data signal and vice versa in a data communication system such as the T1 carrier system that operates with a DS-1 signal. Column 1, lines 9-41. In order to maintain maximum throughput on a T1 line, the one's density requirement must be complied with. Accordingly, a channel bank's Line Interface Unit (LIU) provides one's density control by inserting a one in bit 2 whenever the other bits in the DS word are all zeros. Column 2, lines 30-31.

Applicant respectfully submits that insertion of a one to maintain a certain density requirement in a T1 data communication system does not suggest or allude to sampling a SYNC pulse signal and removing an anomalous condition therein by activating appropriate SYNC correct control logic. The combined teachings of the *Price* and *Meagher* references fail to teach or suggest all the limitations of the base claim 10 as required under MPEP §2143. Additionally, even if the teachings of the applied references were to be combined, there cannot be a reasonable expectation of successfully obtaining Applicant's claimed invention because the operating conditions of a T1 transmission line (in the *Meagher* reference) are vastly different from those of the asynchronous subsystems within a computer as disclosed in the *Price* reference.

PATENT APPLICATION
DOCKET NO.: 10012773-1

Accordingly, Applicant respectfully submits that the base claim 10 is allowable over the *Price* and *Meagher* references.

Analysis with respect to Base Claim 14:

The following comments were provided in particular reference to the §103 rejection of the base claim 14:

As per claim 14 *Price* (US 5450458) discloses sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67); determining a clock state indicative of a phase difference between said first and second clock signals (figure 7 block 74 column 7 lines 46-48); *Price* doesn't disclose re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state. *Kurd* discloses re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 5 column 5 lines 10-16). *Price* and *Kurd* teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by *Kurd* with the SYNC pulse signal disclosed by *Price*. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (*Kurd* column 1 lines 11-18).

PATENT APPLICATION
DOCKET NO.: 10012773-1

Again, Applicant respectfully traverses the pending §103 rejection of the base claim 14 as applied above and offers the following arguments in support. As discussed previously, the applied language of the *Price* reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to sampling a SYNC pulse signal. Further, the applied language at column 7, lines 46-48 does not teach, suggest or allude to determining a clock state indicative of a phase difference between first and second clock signals. Rather, a frequency synthesizer with waveform sequencer 74 (see Figure 7) is described therein which is in data communication with CPU 58 via a First SYNC bus 78 and in data communication with Memory Controller 62 via a Second SYNC bus 82. The function of the waveform sequencer is further described in reference to a particular embodiment of waveform sequencer 132 shown in Figure 8. As shown therein, waveform sequencer 132 generates multiple frequency clocks, CLK 1 and CLK 2, as well as multiple SYNC pulses. See also column 9, lines 15-30. Applicant accordingly submits that the applied language provides no suggestion of determining a clock state indicative of a phase difference between first and second clock signals as claimed.

On the other hand, application of the *Kurd* reference does not cure the deficiency of the *Price* reference when applied in

PATENT APPLICATION
DOCKET NO.: 10012773-1

combination therewith. Although it is provided in *Kurd* that an adjusted reference clock is obtained by delaying a reference clock signal in accordance with a first count (column 5, lines 10-16), there is no teaching or suggestion with respect to determining a clock state and re-positioning a SYNC pulse signal based on the clock state. Accordingly, even if the two references were to be combined, they fail to teach or suggest all the limitations of the base claim 14.

Analysis with respect to Dependent Claims:

Dependent claims 2-9 depend from the base claim 1 and introduce additional limitations therein. Dependent claims 11-13 depend from the base claim 10 and introduce additional limitations therein. Finally, dependent claims 15-19 depend from the base claim 14 and introduce additional limitations therein. Accordingly, these dependent claims are allowable over the *Price*, *Kurd* and *Meagher* references, in any combination, based on the foregoing analysis regarding their respective base claims.

Also, as pointed out earlier, three other references, the *Kim* reference, the *Langendorf* reference and the *Magro* reference, are applied in one or more combinations with the references used against the base claims in rejecting some of the pending dependent

PATENT APPLICATION
DOCKET NO.: 10012773-1

claims. The Kim reference is directed to a delay locked loop of a memory device (DRAM). The Langendorf reference is directed to a programmable secondary clock generator. The Magro reference is directed to synchronizing data between differing clock domains. Applicant respectfully submits that these additional references are of no avail when applied in combination with one or more of the Price, Kurd and Meagher references against the base claims. Accordingly, it is believed that the dependent claims are also allowable over the entire art made of record.


PATENT APPLICATION
DOCKET NO.: 10012773-1

SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the present invention, as now defined by the independent claims, and in further view of the above amendments and remarks, reconsideration of the Action and allowance of the present invention are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: 4/11/2005


Shreen K. Danamraj
Registration No. 41,696

Correspondence Address

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Please direct telephone calls to:
T. Grant Ritz
(970) 898-0697